

The diagram illustrates a Transceiver system, labeled 1 and 2. The Transmitter (1) is enclosed in a dashed box and includes a Front Encoder, an FFT block (10), an Add CP block (11), a Parallel to Serial block (12), a D/A block (13), and a Transmit Analog HP Filter (14). The Receiver (2) is also enclosed in a dashed box and includes a Receive Analog HP Filter (20), an A/D block (21), a Delay block (22), a Time Domain Equalizer (TED) block (23), a Summing junction (25), a Serial to Parallel block (26), a Remove CP block (27), and an FFT block (28). A feedback loop from the TED block (23) passes through a Tail estimation block (24) and returns to the Summing junction (25). The Transmitter and Receiver are connected to a Channel (30).

Fig. 1